REMARKS

No claims have been amended, added, or canceled. Thus, Claims 1-36 are pending in the application.

I. SUMMARY OF THE REJECTIONS

Claims 1-36 have been rejected under the judicially created doctrine of double patenting over Claims 1-18 of U.S. Patent No. 6,678,877.

Claims 1 and 19 have been rejected under 35 U.S.C. § 102(e) as allegedly being unpatentable over U.S. Patent Number 5,903,886 by Heimlich et al. ("*Heimlich*").

Claims 2-18 and 20-36 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Heimlich in view of U.S. Patent Number 6,195,613 by Roy et al. ("*Roy*").

The rejections are traversed, respectfully.

II. RESPONSE TO REJECTIONS BASED ON THE PRIOR ART

Double Patenting Rejection

A terminal disclaimer has been filed herewith to obviate the double patenting rejection of Claims 1-36 over Claims 1-18 of U.S. Patent No. 6,678,877. Applicants respectfully request that the double patenting rejection of Claims 1-36 over Claims 1-18 of U.S. Patent No. 6,678,877 be withdrawn.

Rejections Under 35 U.S.C. 102(e)

Claim 1 requires, *inter alia*, "receiving said user-specified functional requirements **over a network** from a client." Although Heimlich's col. 7, lines 36-42 disclose that information is provided by a user in the form of previous examples of task

inputs and corresponding outputs and/or expert knowledge, Heimlich fails to teach or suggest that the user provides such information **over a network**.

On a similar note, Claim 1 requires "delivering to said client **over said network** component information that identifies said components." Although Heimlich's col. 24, lines 63-67 disclose that results of any steps within an emulated process can be output to a user, Heimlich fails to teach or suggest that such information is output **over a network**.

Claim 1 also requires "**automatically determining**, based on said user-specified requirements, **components** and a topology for constructing a particular circuit that is constructable on a circuit board." The Final Office Action asserts that this limitation is disclosed in Heimlich's abstract and col. 10, lines 7-40. Heimlich's abstract discloses:

> The present invention defines a method for emulating an iterated process represented by a series of related tasks and a control mechanism that monitors and enables the iterative execution of those tasks until data associated with the process converges to predetermined goals or objectives. The invention defines a method in which fuzzy neural networks and discreet algorithms are applied to perform the process tasks and in which configurable, reloadable finite state machines are applied to control the execution of those tasks. In particular, the present invention provides a method for emulating the process of designing integrated circuit (IC) applications and printed circuit board (PCB) applications for the purpose of simulating, emulating, analyzing, optimizing and predicting the behavioral and physical characteristics of the application at the earliest possible stage of the process. The invention applies fuzzy neural networks and configurable, reloadable finite state machines to emulate the IC or PCB design process, enabling the invention to emulate the the computer aided design (CAD) tools used to perform the design process tasks as well as the individuals using those tools. By emulating the combination of man and machine performances, the invention can more accurately predict the results of a given task than tools that consider only the machine element. The invention also provides a means to adapt the performance and behavior of any element of the invention using historical data compiled from previous design or manufacturing experiences, allowing the invention to incorporate the knowledge gained from previous designs into current designs.

The abstract does not mention automatically determining components for constructing a circuit. In fact, the word "component" is not even in the abstract. Heimlich's col. 10, lines 7-40 disclose:

> The operation of the virtual tools is supervised and sequenced by the state machine elements of the Tool Manager of FIG. 6, as shown in FIG. 12. The state machine component of the Tool Manager provides the inputs to the virtual tools, monitors its progress toward completion by way of the Events in FIG. 11, and manages the virtual tools' outputs. The user interface component of the Tool Manager provides interaction with the user during operational and training modes of the invention. Upon completion, the outputs are stored such that they can be accessed by virtual tools to be executed later in the process emulation. The state machine element of the tool manager is implemented, as a dynamically configurable and reloadable finite state machine (FSM), where the states are the virtual tools representing the tasks of the process and the events are steps linking the process tasks. The combination of FSM and fuzzy neural net based MME creates a generic methodology and architecture for emulating a process in software (FIGS. 13A and 13B). Element Process A of FIG. 13A illustrates the entire process which is to be performed and for which specifications are known. FIGS. 13A and 13B are is derived from FIG. 9 in its entirety and its tasks have been subdivided into Element Subprocess A and Element Step 1. This illustration of the invention in its most general application shows that Subprocess A is embodied as Element Software Tool B and is made available to the Element man of Element Step 1 in the form of Element machine. Element Subprocess A is representative of one or any number of tasks which follow Element Step 1 and which may need to be iterated because the criteria for completion of the process, or identifiable tasks, collections of tasks, or subprocesses, are not met in the current iteration.

Although the above passage refers to "components," the components referred to are components of a Tool Manager rather than components of a circuit. The Tool Manager is not a circuit. Heimlich's col. 10, lines 7-40, do not mention automatically determining components for constructing a circuit. Instead, Heimlich apparently discloses emulating a circuit design process, which does not include automatically determining components of the circuit.

It appears that Heimlich actually discloses that "Schematic Parser B" is simply an interface that translates an already-defined schematic from one format to another (col. 13,

lines 45-55). The schematic parser apparently "translates an electrical design schematic into a connectivity matrix, where the electrical design schematic **identifies components**" (col. 27, lines 40-42). Thus, it seems that the electrical design schematic that is provided to the schematic parser **already** identifies components of a circuit; therefore, there is no need to automatically determine such components. Although Heimlich discloses that "the pseudo placement section determines routing channels, component size and placement," (col. 27, lines 43-45) Heimlich fails to teach or suggest automatically determining components themselves.

Claim 1 also requires "determining components that have operational values such that, when said components are arranged according to said topology to form said particular circuit, the particular circuit satisfies said user-specified functional requirements." Thus, Claim 1 requires the determination of components based on topology and user-specified requirements. Although Heimlich discloses that a "pseudo placement section" determines component size, as discussed above, Heimlich fails to teach or suggest determining the components themselves. Although Heimlich discloses that an "electromagnetic translator section" determines electromagnetic parameters (col. 28, lines 15-18), the determination of such parameters is not the same as the determination of components of a circuit. Electromagnetic parameters are not components. Although Heimlich discloses that information related to previous microprocessor design experiences can allow virtual tools to predict characteristics of next generation devices (col. 25, lines 50-58), Heimlich does not teach or suggest that such characteristics include the components of such devices. Because Heimlich does not even teach or suggest the automatic determination of components, it logically follows

that Heimlich also fails to teach or suggest the automatic determination of components based on topology and user-specified requirements.

For at least the above reasons, Claim 1 is patentable over Heimlich. Claim 19 is computer-readable medium counterpart of Claim 1. Therefore, for at least the same reasons that Claim 1 is patentable over Heimlich, Claim 19 is also patentable over Heimlich.

Rejections under 35 U.S.C. 103(a)

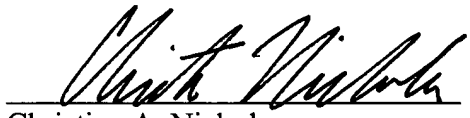
Claims 2-18 depend from Claim 1. Claims 20-36 depend from Claim 19. As discussed above, Claims 1 and 19 include multiple limitations that are not taught or suggested by Heimlich individually. The Final Office Action does not even allege that these limitations of Claims 1 and 19 are taught or suggested by Roy. Therefore, even assuming, *arguendo*, that Heimlich and Roy could be combined, the combination does not teach or suggest the limitations of Claims 1 and 19. Because dependent claims contain the limitations of the claims on which they depend, Claims 2-18 and 20-36 are also patentable over Heimlich and Roy, taken individually or in combination.

III. CONCLUSION

For the reasons set forth above, it is respectfully submitted that all of the pending claims are now in condition for allowance. Therefore, the issuance of a formal Notice of Allowance is believed next in order, and that action is most earnestly solicited.

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Respectfully submitted,
HICKMAN PALERMO TRUONG & BECKER LLP



Christian A. Nicholes
Reg. No. 50,266

1600 Willow Street
San Jose, CA 95125
(408) 414-1080, ext. 207
Date: October 14, 2004
Facsimile: (408) 414-1076

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on 10/14/04 by Judy Panadashi